

Amendments to the Claims

1. (Currently Amended) A circuit arrangement for controlling a first terminal and a second terminal of a ~~preferably~~ contactless integrated circuit, ~~particularly for testing a CMOS circuit,~~ characterized in that the circuit arrangement (100) comprises:

- at least a control stage (10) which generates, from an external modulation signal (M_0) and an external clock signal (C_0)
 - a first modulation signal (M_1);
 - a second modulation signal (M_2) which is temporally shifted with respect to the first modulation signal (M_1);
 - a ~~preferably~~ symmetrical first clock signal (C_1); and
 - a ~~preferably~~ symmetrical second clock signal (C_2) which is inverted with respect to the first clock signal (C_1);
- at least a first driver stage (40),
 - which is connected to a first power supply voltage ($U_{dd,1}$) amplitude-modulated by the first modulation signal (M_1) and to a first reference potential ($U_{ss,1}$) and
 - ~~can be~~ which is impressed with the first clock signal (C_1) in such a way that the output voltage ($U_{o,1}$) of the first driver stage (40), ~~which can be~~ applied to the first terminal of the integrated circuit, temporally assumes the value of the amplitude-modulated first power supply voltage ($U_{dd,1}$)

- and temporally the value of the first reference potential ($U_{ss,1}$) in accordance with the clock of the first clock signal (C_1); and
- at least a second driver stage (50),
 - which is connected to a second power supply voltage ($U_{dd,2}$) amplitude-modulated by the second modulation signal (M_2) and to a second reference potential ($U_{ss,2}$) and
 - ~~can be~~ which is impressed with the second clock signal (C_2) in such a way that the output voltage ($U_{o,2}$) of the second driver stage (50), ~~which can be~~ applied to the second terminal of the integrated circuit, temporally assumes the value of the amplitude-modulated second power supply voltage ($U_{dd,2}$) and temporally the value of the second reference potential ($U_{ss,2}$) in accordance with the clock of the second clock signal (C_2).

2. (Original) A circuit arrangement as claimed in claim 1, characterized in that the control stage (10) comprises:

- a modulation signal input (12) provided for the external modulation signal (M_0);
- a clock signal input (14) provided for the external clock signal (C_0);
- a first logic gate circuit, particularly an exclusive-OR circuit (22) connected to the clock signal input (14) and supplying the first clock signal (C_1) from its output (22o);
- a second logic gate circuit, particularly an exclusive-OR circuit (32) arranged parallel to the first logic gate circuit (22) and connected to the clock signal input (14)

and supplying the second clock signal (C_2) which is inverted with respect to the first clock signal (C_1) from its output (32o);

- a first delay unit (24) delaying the first clock signal (C_1) by a first time interval (Δt_1) and connected to the output (22o) of the first logic gate circuit (22);
- a second delay unit (34) delaying the second clock signal (C_2) by a second time interval (Δt_2) and connected to the output (32o) of the second logic gate circuit (32);
- a first D(elay)-flipflop unit (26);
 - whose clock input (26c) is connected to the output (24o) of the first delay unit (24);
 - whose D input (26m) is connected to the modulation signal input (12); and
 - whose Q output (26o) supplies the first modulation signal (M_1); and
- a second D(elay)-flipflop unit (36),
 - whose clock input (36c) is connected to the output (34o) of the second delay unit (34);
 - whose D input (36m) is connected to the modulation signal input (12); and
 - whose Q output (36o) supplies the second modulation signal (M_2) which is temporally shifted with respect to the first modulation signal (M_1).

3. (Original) A circuit arrangement as claimed in claim 2, characterized in that the first temporal delay (Δt_1) generated in the first delay unit (24) and the second temporal delay (Δt_2) generated in the second delay unit (34) have approximately equal temporal lengths.

4. (Previously Amended) A circuit arrangement as claimed in claim 2, characterized in that the first temporal delays (Δt_1) generated in the first delay unit (24) and/or the second temporal delays (Δt_2) generated in the second delay unit (34) can each be built up with gate delay times.

5. (Previously Amended) A circuit arrangement as claimed claim 1, characterized in that the second modulation signal (M_2) is temporally shifted with respect to the first modulation signal (M_1) by approximately half a clock period of the external clock signal (C_0).

6. (Currently Amended) A circuit arrangement as claimed in claim 1, characterized in that

- the first driver stage (40) comprises:
 - a clock signal input (42c) provided for the first clock signal (C_1);
 - a modulation signal input (42m) provided for the first modulation signal (M_1) for controlling the switching of each modulation voltage (U_{unmod} or U_{mod}) to the amplitude-modulated first power supply voltage ($U_{dd,1}$);
 - a first electronic switch (44);

- a second electronic switch (46) ~~arranged behind~~ coupled to the first switch (44); and
- an output (48) provided for the first output signal comprising the output voltage ($U_{o,1}$),
 - wherein ~~the~~ a control means (442) of the first switch (44) and ~~the~~ a control means (462) of the second switch (46) are each connected to the clock signal input (42c);
 - ~~the~~ a power supply voltage-sided contact (444) of the first switch (44) is connected to the amplitude-modulated first power supply voltage ($U_{dd,1}$),
 - ~~the~~ a reference potential-sided contact (464) of the second switch (46) is connected to the first reference potential ($U_{ss,1}$), and
 - ~~the~~ an output voltage-sided contact (446) of the first switch (44) and ~~the~~ an output voltage-sided contact (466) of the second switch (46) are connected together and to the output (48), and
- in that the second driver stage (50) comprises:
 - a clock signal input (52c) provided for the second clock signal (C_2);
 - a modulation signal input (52m) provided for the second modulation signal (M_2) for controlling the switching of each modulation voltage (U_{unmod} or U_{mod}) to the amplitude-modulated second power supply voltage ($U_{dd,2}$);

- a first electronic switch (54);
- a second electronic switch (56) ~~arranged behind~~ coupled to the first switch (54); and
- an output (58) provided for the second output signal comprising the output voltage ($U_{o,2}$),
 - wherein ~~the~~ a control means (542) of the first switch (54) and ~~the~~ a control means (562) of the second switch (56) are each connected to the clock signal input (52c),
 - ~~the~~ a power supply voltage-sided contact (544) of the first switch (54) is connected to the amplitude-modulated second power supply voltage ($U_{dd,2}$),
 - ~~the~~ a reference potential-sided contact (564) of the second switch (56) is connected to the second reference potential ($U_{ss,2}$), and
 - ~~the~~ an output voltage-sided contact (546) of the first switch (54) and ~~the~~ an output voltage-sided contact (566) of the second switch (56) are connected together and to the output (58).

7. (Original) A circuit arrangement as claimed in claim 6, characterized in that the relevant first electronic switch (44; 54) and/or the relevant second electronic switch (46; 56) are formed as transistors.

8. (Previously Amended) A circuit arrangement as claimed in claim 1, characterized in that the first driver stage (40) and the second driver stage (50) are complementary with respect to each other.

9. (Previously Amended) A circuit arrangement as claimed in claim 1, characterized in that the first power supply voltage ($U_{dd,1}$) and the second power supply voltage ($U_{dd,2}$) have different values.

10. (Previously Amended) A circuit arrangement as claimed in claim 1, characterized in that the first reference potential ($U_{ss,1}$) and the second reference potential ($U_{ss,2}$) are at least approximately equally large.

11. (Previously Amended) A circuit arrangement as claimed in claim 1, characterized in that the first reference potential ($U_{ss,1}$) and/or the second reference potential ($U_{ss,2}$) are the earth potential or the ground potential.

12. (Currently Amended) A ~~preferably~~ contactless integrated circuit, particularly a CMOS circuit controlled and particularly tested by at least a circuit arrangement (100) as claimed in any one of claim 1.

13. (Original) An integrated circuit as claimed in claim 12, characterized in that the integrated circuit is arranged on a wafer of a carrier substrate of a semiconducting or insulating material.